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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/643,895	08/18/2000	Quinn A. Jacobson	SUN-P4914	8680

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MARTINE PENILLA & GENCARELLA, LLP
710 LAKEWAY DRIVE
SUITE 200
SUNNYVALE, CA 94085

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/643,895	JACOBSON ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 20-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 20-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 20-25, and new claims 26-27 have been considered. New claims 26-27 have been added as per Applicant's request. Claims 1, 3 and 22 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 27 April 2006.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 and 22-23 are rejected under 35 U.S.C. 103(a) as being taught by Moyer et al., U.S. Patent Number 5,375,216 (herein referred to as Moyer) in view of Brodnax et al., U.S. Patent Number 5,562,380 (herein referred to as Brodnax).

5. Referring to claims 1 and 22, taking claim 1 as exemplary, Moyer has taught a processor, comprising:

a. At least one register file (Moyer column 5, lines 34-39 and Figure 1, element 32);

b. At least one execution unit coupled to the at least one register file (Moyer column 5, lines 34-39 and Figure 1, elements 42, 32, and 27), the at least one register file being available to programs for temporarily storing operands and results (Moyer column 6, lines 3-15 and Figure 1, element 32);

c. At least one bypass circuit operatively coupled to said at least one register file and said at least one execution unit (Moyer column 5, line 62 to column 6, line 15 and Figure 1, elements 34), said at least one bypass circuit capable of arbitrating access by said at least one execution unit to said at least one register file (Moyer column 5, line 62 to column 6, line 15 and Figure 1, elements 34); and

d. A backing register file operatively coupled to said at least one register file (Moyer column 5, lines 34-39; column 6, lines 50-64; Figure 1, element 24; Figure 5; Figure 6; and Figure 7), said backing register file being inaccessible to the at least one execution unit (Moyer column 5, lines 34-39; column 6, lines 50-64; and Figure 1, element 24) and, in at least one mode, is always visible outside the processor and available to the programs at any privilege level (Moyer column 3, lines 6-28; column 3, line 66 to column 4, line 8; column 4, lines 35-54; and Figure 1). In regards to Moyer, the backing register file is the data cache unit, which is only accessible via the load/store unit. The execution units do not have access to the data cache unit, and there are instructions that manipulate the cache control.

6. Moyer has not taught a backing register file comprising a plurality of registers and the backing register file is directly accessible to instructions. Brodnax has taught a backing register file comprising a plurality of registers and the backing register file is directly accessible to instructions (Brodnax column 3, lines 21-51; Figure 2; and Figure 3). A person of ordinary skill in the art at the time the invention was made, and as taught by Brodnax, would have recognized that having the backing register file, aka shadow register file, accessible directly by instructions

allows the data in the general register file to be loaded and unloaded from the shadow register file in response to a command sent by the processor, thereby improving fault-tolerance and error correction of the system (Brodnax column 1, lines 42 to column 2, line 11). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the shadow registers of Brodnax in the device of Moyer to improve fault tolerance and error correction.

7. Claim 22 has similar limitations to claim 1 and is rejected for the reasons set forth above. Claim 22 differs only in that it is for the backing register file rather than the entire processor, as in claim 1.

8. Referring to claims 2 and 23, taking claim 2 as exemplary, Moyer has taught wherein the at least one register file comprises a plurality of register files (Moyer column 6, lines 3-15 and Figure 1), each execution unit of the at least one execution unit being operably connected to only one register file of said plurality of register files (Moyer column 5, lines 34-39; column 6, lines 3-15; and Figure 1), said backing register file bring operably connected to each register file of said plurality of register files thereby allowing a transfer of values from any designated location in any designated register file of said plurality of register files to any designated location in said backing register file, and from any designated location in said backing register file to any designated location in any designated register file of said plurality of register files (Moyer column 6, lines 50-64; Figure 1; Figure 5; Figure 6; and Figure 7).

9. Claim 23 has similar limitations to claim 2 and is rejected for the reasons set forth above. Claim 23 differs only in that it is for the backing register file rather than the entire processor, as in claim 2.

10. Referring to claim 3, Moyer has taught a first connection operably connected to said backing register file from the at least one register file (Moyer column 5, lines 24-39; column 6, lines 50-64; and Figure 1), the first connection comprising a full set of address and data lines allowing the backing register file to address and access individual registers and each of the at least one register file (Brodnax column 3, lines 21-51; Figure 2; and Figure 3); and a second connection operably connected to a main memory from the said backing register file, the connection circuit providing a series of connections and interfaces placing the backing register file in communication with the main memory (Moyer column 5, lines 24-39; column 6, lines 50-64; and Figure 1).

11. Claims 20-21 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer et al., U.S. Patent Number 5,375,216 (herein referred to as Moyer) in view of Brodnax et al., U.S. Patent Number 5,562,380 (herein referred to as Brodnax), as applied to claim 1, in view of Wikipedia "Register Window" (herein referred to as Wikipedia).

12. Referring to claims 20-21 and 24-25, Moyer has not taught

a. Wherein the backing register file is further operable in a windowing mode wherein the backing register file mimics register windowing functionality wherein less than all the registers in the backing register file is accessible to a particular process at one time (Applicant's claims 20 and 24).

b. Wherein the backing register file operates in one of the windowing mode or the native mode depending upon instructions in a current instruction stream of a current process (Applicant's claims 21 and 25),

c. Wherein when the instruction stream includes register windowing instructions, the backing register file operates in the windowing mode, and when the instruction stream does not include register windowing instructions then the backing register file operates in the native mode (Applicant's claims 21 and 25).

13. Wikipedia has taught register windowing when there is a procedure call present (Wikipedia search term: register window). A person of ordinary skill in the art at the time the invention was made would have recognized that register windowing is reduces the amount of time necessary to save data to memory when a procedure call is present, since it does not require the data in the register to be moved from the registers to memory, thereby improving performance (Wikipedia search term: register window). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the register windows of Wikipedia in the device of Moyer to improve performance.

14. Claims 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer et al., U.S. Patent Number 5,375,216 (herein referred to as Moyer) in view of Brodnax et al., U.S. Patent Number 5,562,380 (herein referred to as Brodnax), as applied to claims 1 and 22, in view of Wikipedia "Register Window" (herein referred to as Wikipedia). Moyer has not taught such that each of the plurality of registers is accessible at random using a uniquely assigned address. InstantWeb has taught using registers. A person of ordinary skill in the art at the time the invention was made, and as taught by InstantWeb, would have recognized that a register faster and typically can read two register and write to a register all in a single cycle (InstantWeb "register"), thereby increasing speed of the processor. Therefore, it would have been obvious to

a person of ordinary skill in the art at the time the invention was made to incorporate the registers of InstantWeb in the device of Moyer to increase processor speed.

Response to Arguments

15. Applicant's arguments with respect to claims 1-3 and 20-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
9 July 2006

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100